PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P32927-P0	FOR FURTHER ACTION See Form PCT/IPEA/416	
International application No. PCT/JP2004/012246	International filing date *(day/month/year)* 19 August 2004	Priority date *(day/month/year)* 29 August 2003
International Patent Classification (IPC) or national classification and IPC Int. Cl.⁷ H03M13/15		
Applicant Matsushita Electric Industrial Co., Ltd.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of ___3___ sheets, including this cover sheet.

3. This report is also accompanied by ANNEXES, comprising:

a ☒ *(sent to the applicant and to the International Bureau)* a total of ___5___ sheets, as follows:

☒ sheets of the description, claims and /or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).

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4. This report contains indications relating to the following items:

☒ I Basis of the report

☐ II Priority

☐ III Non-establishment of opinion with regard to novelty, inventive step or industrial applicability

☐ IV Lack of unity of invention

☒ V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

☐ VI Certain documents cited

☐ VII Certain defects in the international application

☐ VIII Certain observations on the international application

Date of submission of the demand 29 June 2005	Date of completion of this report 08 September 2005
Name and mailing address of the IPEA/JP **Japanese Patent Office**	Authorized officer
Facsimile No.	Telephone No.

ATTACHMENT G

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY	International application No. **PCT/JP2004/012246**

Ⅰ. Basis of the report

1. With regard to the language, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

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2. With regard to the elements of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed " and are not annexed to this report)*:

☒ the description:
pages 1-23   , as originally filed/furnished

☒ the claims:
Nos. 3, 4, 6, 7, 12-14, as originally filed/furnished
Nos. 1, 8   , received by this Authority on 29 June 2005

☒ the drawings:
pages 1-15   , as originally filed/furnished

3. ☒ The amendments have resulted in the cancellation of:

☒ the claims, Nos. 2, 5, 9-11

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/012246

V. Reasoned statement under Rule 12 (PCT Article 35(2)) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)
Claims   1,3,4,6-8,12-14   YES
Claims   NONE   NO

Inventive Step(IS)
Claims   1,3,4,6-8,12-14   YES
Claims   NONE   NO

Industrial Applicability (IA)
Claims   1,3,4,6-8,12-14   YES
Claims   NONE   NO

2. CITATIONS AND EXPLANATIONS (Rule70.7)

Reference 1: JP 2001-23316 A (Hitachi,Ltd.) 2001.01.26, whole text, whole figure
Reference 2: JP 2001-292066 A (Sanyo Electric Co.,Ltd.) 2001.10.19, paragraphs [0001]-[0035], figures 17-25 & US 2001/0014960 A1 & CA 1318836 A

Claims 1-14

Reference 1 cited in the International Search Report discloses an error detection apparatus which performs error correction and error detection simultaneously on a target code string comprising plural sectors, each sector comprising matrix data, which apparatus includes a means for updating the result of error detection code operation on the basis of the result of error correction. Further, it is also described that scrambles are removed on the basis of the updated result of error detection code operation.

Reference 2 cited in the International Search Report (particularly refer to description relating to [Fig.23]) discloses a means for performing offset calculation (corresponding to "skip operation") when a target code string comprising plural sectors, each sector comprising matrix data, is inputted in discontinuous data arrangement (PO direction).

However, the References 1 and 2 neither describe nor suggest that "the error detection code skip operation circuit receives error detection codes of target code strings which have been inputted by the last time, and performs an individual skip operation which skips a predetermined number of bytes according to the column positions where the data exist, in the last row in the sector, and the individual skip operation is carried out by utilizing plural times the result of skip operation that is executed for a specific column position among the column positions where the data exist", which construction is peculiar to the present invention.